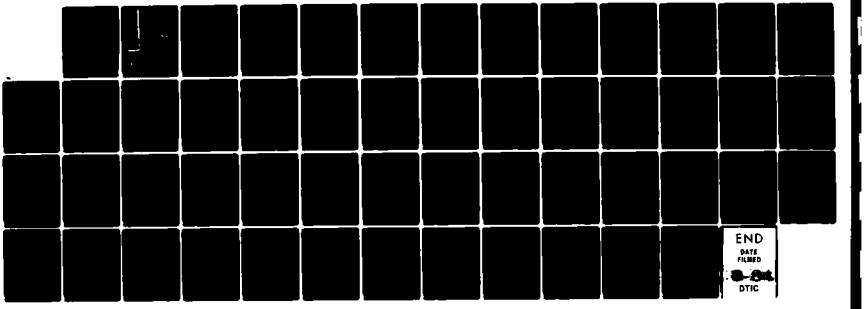
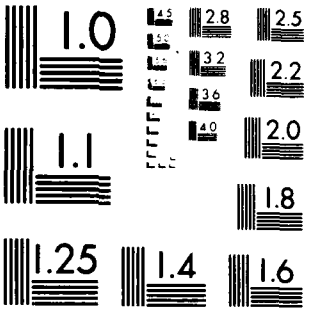
AD-A142 782 PROCEEDINGS PAPERS OF THE AFSC (AIR FORCE SYSTEMS COMMAND) AVIONICS STAND..(U) AERONAUTICAL SYSTEMS DIV WRIGHT-PATTERSON AFB OH DIRECTORATE O..

1/1

UNCLASSIFIED C A PORUBCANSKY NOV 82 F/G 9/2 NL





ASD(ENA)-TR-82-5031
VOLUME VII

(2)

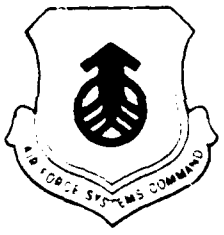
2nd AFSC STANDARDIZATION CONFERENCE

COMBINED PARTICIPATION BY:
DOD-ARMY-NAVY-AIR FORCE-NATO

30 NOVEMBER - 2 DECEMBER 1982
TUTORIALS: 29 NOVEMBER 1982

DAYTON CONVENTION CENTER
DAYTON, OHIO

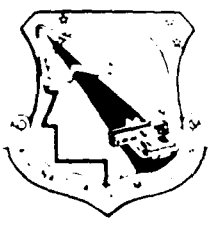
SPONSORED BY



TUTORIAL

MIL-STD-1750
16 BIT INSTRUCTION SET ARCHITECTURE

HOSTED BY



NOTICE

When Government drawings, specifications, or other data are used for any purpose other than in connection with a definitely related Government procurement operation, the United States Government thereby incurs no responsibility nor any obligation whatsoever; and the fact that the government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data, is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture use, or sell any patented invention that may in any way be related thereto.

This report has been reviewed by the Office of Public Affairs (ASD/PA) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nations.

This technical report has been reviewed and is approved for publication.

Jeffery L Pesler

JEFFERY L. PESLER
Vice Chairman
2nd AFSC Standardization Conference

E C Gangl

ERWIN C. GANGL
Chief, Avionics Systems Division
Directorate of Avionics Engineering

FOR THE COMMANDER

Robert P Lavoie

ROBERT P. LAVOIE, COL, USAF
Director of Avionics Engineering
Deputy for Engineering

"If your address has changed, if you wish to be removed from our mailing list, or if the addressee is no longer employed by your organization please notify ASD/ENAS *, W-PAFB, OH 45433 to help us maintain a current mailing list".*

Copies of this report should not be returned unless return is required by security considerations, contractual obligations, or notice on a specific document.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER: ASD(ENA)-TR-82-5031, VOLUME VII	2. GOVT ACCESSION NO.: AD-A142 782
	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle): Proceedings Papers of the Second AFSC Avionics Standardization Conference	5. TYPE OF REPORT & PERIOD COVERED: Final Report, 29 November - 2 December 1982
	6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s): Editor: Cynthia A. Porubcansky	8. CONTRACT OR GRANT NUMBER(s)
9. PERFORMING ORGANIZATION NAME AND ADDRESS: HQ ASD/ENAS, Wright-Patterson AFB OH 45433	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS: HQ ASD/ENA, Wright-Patterson AFB OH 45433	12. REPORT DATE: November 1982
	13. NUMBER OF PAGES
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Same as Above	15. SECURITY CLASS. (of this report): Unclassified
	15a. DECLASSIFICATION DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

N/A

18. SUPPLEMENTARY NOTES

N/A

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Computer Instruction Set Architecture, Multiplexing, Compilers, Support Software, Data Bus, Rational Standardization, Digital Avionics, System Integration, Stores Interface, Standardization, MIL-STD-1553, MIL-STD-1589 (JOVIAL), MIL-STD-1750, MIL-STD-1760, MIL-STD-1815 (ADA), MIL-STD-1862 (NEBULA).

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This is a collection of UNCLASSIFIED papers to be distributed to the attendees of the Second AFSC Avionics Standardization Conference at the Convention Center, Dayton, Ohio. The scope of the Conference includes the complete range of DoD approved embedded computer hardware/software and related interface standards as well as standard subsystems used within the Tri-Service community and NATO. The theme of the conference is "Rational Standardization". Lessons learned as well as the pros and cons of standardization are highlighted.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

This is Volume 7

Volume 1	Proceedings pp. 1-560
Volume 2	Proceedings pp. 561-1131
Volume 3	Governing Documents
Volume 4	MIL-STD-1553 Tutorial
Volume 5	MIL-STD-1589 Tutorial
Volume 6	MIL-STD-1679 Tutorial
Volume 7	MIL-STD-1750 Tutorial
Volume 8	MIL-STD-1815 Tutorial
Volume 9	Navy Case Study Tutorial

PROCEEDINGS OF THE

2nd AFSC STANDARDIZATION CONFERENCE

30 NOVEMBER - 2 DECEMBER 1982

DAYTON CONVENTION CENTER
DAYTON, OHIO

Sponsored by:

Air Force Systems Command

Hosted by:

Aeronautical Systems Division

FOREWORD

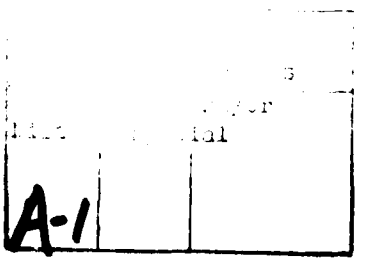
THE UNITED STATES AIR FORCE HAS COMMITTED ITSELF TO "STANDARDIZATION." THE THEME OF THIS YEAR'S CONFERENCE IS "RATIONAL STANDARDIZATION," AND WE HAVE EXPANDED THE SCOPE TO INCLUDE US ARMY, US NAVY AND NATO PERSPECTIVES ON ONGOING DOD INITIATIVES IN THIS IMPORTANT AREA.

WHY DOES THE AIR FORCE SYSTEMS COMMAND SPONSOR THESE CONFERENCES? BECAUSE WE BELIEVE THAT THE COMMUNICATIONS GENERATED BY THESE GET-TOGETHERS IMPROVE THE ACCEPTANCE OF OUR NEW STANDARDS AND FOSTERS EARLIER, SUCCESSFUL IMPLEMENTATION IN NUMEROUS APPLICATIONS. WE WANT ALL PARTIES AFFECTED BY THESE STANDARDS TO KNOW JUST WHAT IS AVAILABLE TO SUPPORT THEM: THE HARDWARE; THE COMPLIANCE TESTING; THE TOOLS NECESSARY TO FACILITATE DESIGN, ETC. WE ALSO BELIEVE THAT FEEDBACK FROM PEOPLE WHO HAVE USED THEM IS ESSENTIAL TO OUR CONTINUED EFFORTS TO IMPROVE OUR STANDARDIZATION PROCESS. WE HOPE TO LEARN FROM OUR SUCCESSES AND OUR FAILURES; BUT FIRST, WE MUST KNOW WHAT THESE ARE AND WE COUNT ON YOU TO TELL US.

AS WE DID IN 1980, WE ARE FOCUSING OUR PRESENTATIONS ON GOVERNMENT AND INDUSTRY EXECUTIVES, MANAGERS, AND ENGINEERS AND OUR GOAL IS TO EDUCATE RATHER THAN PRESENT DETAILED TECHNICAL MATERIAL. WE ARE STRIVING TO PRESENT, IN A SINGLE FORUM, THE TOTAL AFSC STANDARDIZATION PICTURE FROM POLICY TO IMPLEMENTATION. WE HOPE THIS INSIGHT WILL ENABLE ALL OF YOU TO BETTER UNDERSTAND THE "WHY'S AND WHEREFORE'S" OF OUR CURRENT EMPHASIS ON THIS SUBJECT.

MANY THANKS TO A DEDICATED TEAM FROM THE DIRECTORATE OF AVIONICS ENGINEERING FOR ORGANIZING THIS CONFERENCE; FROM THE OUTSTANDING TECHNICAL PROGRAM TO THE UNGLAMOROUS DETAILS NEEDED TO MAKE YOUR VISIT TO DAYTON, OHIO A PLEASANT ONE. THANKS ALSO TO ALL THE MODERATORS, SPEAKERS AND EXHIBITORS WHO RESPONDED IN SUCH A TIMELY MANNER TO ALL OF OUR PLEAS FOR ASSISTANCE.

ROBERT P. LAVOIE, COL, USAF
DIRECTOR OF AVIONICS ENGINEERING
DEPUTY FOR ENGINEERING



DEPARTMENT OF THE AIR FORCE
HEADQUARTERS AIR FORCE SYSTEMS COMMAND
ANDREWS AIR FORCE BASE DC 20334

28 AUG 1982

REPLY TO ATTN OF: CV

SUBJECT: Second AFSC Standardization Conference

TO: ASD/CC

1. Since the highly successful standardization conference hosted by ASD in 1980, significant technological advancements have occurred. Integration of the standards into weapon systems has become a reality. As a result, we have many "lessons learned" and cost/benefit analyses that should be shared within the tri-service community. Also, this would be a good opportunity to update current and potential "users." Therefore, I endorse the organization of the Second AFSC Standardization Conference.

2. This conference should cover the current accepted standards, results of recent congressional actions, and standards planned for the future. We should provide the latest information on policy, system applications, and lessons learned. The agenda should accommodate both government and industry inputs that criticize as well as support our efforts. Experts from the tri-service arena should be invited to present papers on the various topics. Our AFSC project officer, Maj David Hammond, HQ AFSC/ALR, AUTOVON 858-5731, is prepared to assist.

ROBERT M. BOND, Lt Gen, USAF
Vice Commander

MIL-STD-1750
16 BIT INSTRUCTION SET ARCHITECTURE

Instructor: Jim A. James
Control Data Corporation

ABSTRACT

The MIL-STD-1750 tutorial is intended to aid those newcomers to the 1750 arena including users and implementers. A brief introduction to the Standard is presented followed by an overview of the instruction set architecture (ISA) and concluded with several selected topic discussions. The introduction includes a brief historical background of the Standard, its scope, its flexibilities, its control procedures, and basic definitions used within it. The ISA overview provides comments and notes on the register structures, data and instruction formats, addressing modes, interrupt priorities, and processor initialization. Selected topics from the Standard are elaborated upon including: expanded memory addressing, I/O operations, interrupt sequencing, and faults or exception handling. Time is allocated during the tutorial presentation for questions and answers with the depth of these discussions dependent on interest and time constraints.

BIOGRAPHY

Mr. James is presently Manager of Advanced Technology at the Government Systems Aerospace organization of Control Data Corporation. Mr. James received his BSEE from the University of Wisconsin in 1963 and has been with Control Data in their military computer architecture activities since that time. He has been the principle architect on a history of various computer developments, the latest including the Navy AN/AYK-14 Standard Airborne Computer. He is also presently chairman of the MIL-STD-1750 User's Group Architecture Committee.

MIL-STD-1750 TUTORIAL OUTLINE

- INTRODUCTION
- 1750A ISA OVERVIEW
- SELECTED TOPIC DISCUSSIONS
  - EXPANDED MEMORY ADDRESSING
  - I/O OPERATIONS
  - INTERRUPT SEQUENCING
  - FAULT HANDLING

JIM A. JAMES
M.S. HQM927
CONTROL DATA CORP.
BOX 609
MPLS., MN. 55440
612-853-4882

CONTROL DATA CORPORATION

AA6133 Rev. 11/77 * 79 COC

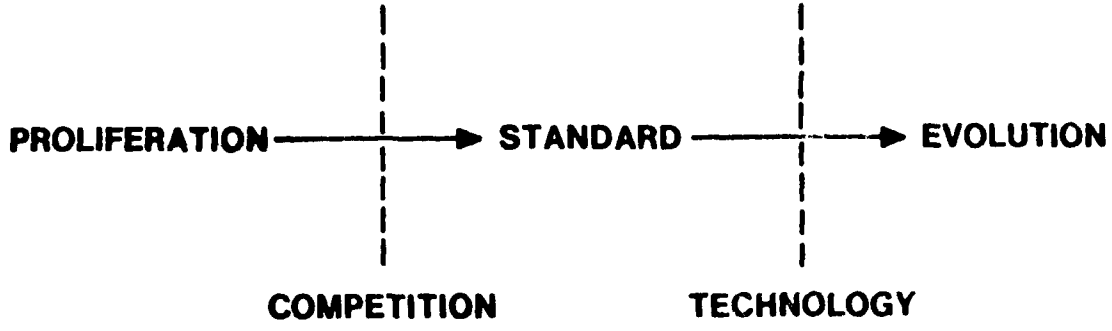
PRINTED IN U.S.A.

MIL-STD-1750A BACKGROUND

- DAIS COMPUTER (WESTINGHOUSE)
  - MIL-STD-1750 (WESTINGHOUSE & SPERRY UNIVAC)
    - MIL-STD-1750A (USER'S GROUP INFLUENCE)
      - MIL-STD-1750A (USAF) DATED 2 JULY 1980
      - MIL-STD-1750A (USAF) PROPOSED NOTICE 1 DATED NOV. 1981

      PRESENTLY ACTIVE VERSION

STANDARDIZATION CHALLENGE



ACQUISITION STRATEGY ?

INSTRUCTION SET ARCHITECTURE (ISA) ASPECTS

(THE COMPUTER AS THE MACHINE LANGUAGE PROGRAMMER SEES IT---
SOFTWARE VIEW OF RESOURCES--MORE THAN JUST THE INSTRUCTION SET)

- INFORMATION ENCODING SCHEME
- REGISTER STRUCTURES
- ADDRESSING
- INTERFACING CONTROL
- INSTRUCTION REPERTOIRE
- CONTEXT DEFINITION AND SEQUENCING

(INDEPENDENT OF IMPLEMENTATION SCHEMES AND TECHNOLOGIES)
(NOT A COMPUTER "SPEC")

COMPUTER SPECIFICATION ISSUES NOT ADDRESSED BY MIL-STD-1750A

- INTEGRATED CIRCUIT TECHNOLOGY
- FORM FACTOR (SIZE, WEIGHT, MOUNTING, ETC.)
- POWER
- PERFORMANCE AND THROUGHPUT
- RELIABILITY
- MAINTAINABILITY
- ELECTRICAL AND MECHANICAL INTERFACE DETAILS (CONNECTORS, PROTOCALS, ETC.)
- ENVIRONMENTAL REQUIREMENTS (THERMAL, NUCLEAR, SALT SPRAY, VIBRATION, ETC.)

(IMPLEMENTATION INDEPENDENT)

MIL-STD-1750A GOALS

- "GOLD STANDARD" BY WHICH MULTIPLE COMPETITIVE IMPLEMENTATIONS OF VARYING TECHNOLOGIES MAY BE DEFINED.
  - EXPLICIT DEFINITION OF RESOURCES
  - UNAMBIGUOUS---NOT OPEN TO INTERPRETATION
- VERIFICATION OR VALIDATION PROCEEDURE WHICH MATCHES "GOLD STANDARD"
- CAPTURE AND RE-USE SUPPORT SOFTWARE---MINIMIZE SUPPORT SOFTWARE PROLIFERATION
- ENABLE PARALLEL DEVELOPMENT OF SOFTWARE AND HARDWARE ON NEW PROGRAMS
- PROVIDE COMPETITIVE IMPLEMENTATION DEVELOPMENT
- CAPTURE EVOLVING IMPLEMENTATION TECHNOLOGY ADVANCEMENTS
- SHARE OPERATIONAL SOFTWARE AMONG SUBSYSTEMS/PLATFORMS???

MIL-STD-1750A APPLICATION TAILORING OPTIONS/FLEXIBILITY AREAS

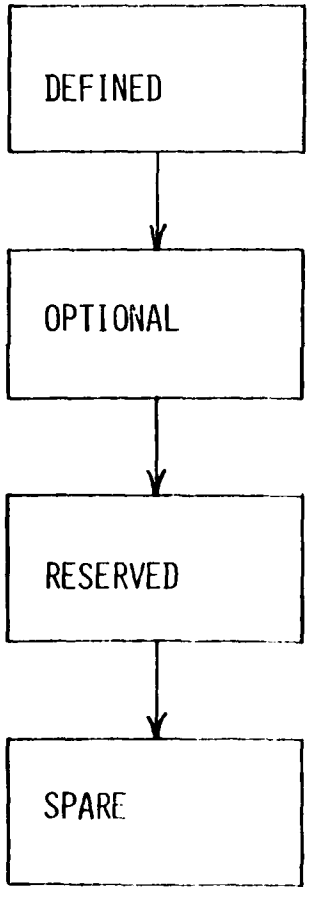
- MEMORY
  - EXPANDED ADDRESSING --- IN "PARTIALS"
  - MEMORY PARITY
  - BLOCK PROTEST
  - START-UP ROM
- I/O
  - INTELLIGENCE LEVELS
  - CHANNEL TYPES, PROTOCALS, ETC.
  - MEMORY INTERFACING SCHEMES
- INTERRUPTS
  - EXPANSION OF SPARES
- BUILT-IN-FUNCTIONS (BIF)
  - ARITHMETIC ALGORITHMS (APPLICATION DEPENDENT)
  - EXECUTIVE FUNCTIONS (IMPROVE RESPONSE AND OVERHEAD PERFORMANCE?)
  - ADD ISA FEATURES
  - ESCAPE ISA

DISCOURAGED

MIL-STD-1750 MILITARY USER'S GROUP (MUG)

- GOVERNMENT/INDUSTRY FORUM ON MIL-STD-1750
- REVIEW RELATED ACTIVITIES
  - STD ISSUES (VIA STANDING COMMITTEES, SPECIAL COMMITTEES, & FULL GROUP)
  - SHARE IMPLEMENTATION INFORMATION
  - SHARE APPLICATION INFORMATION
  - FOCUS ON MATURING MIL-STD-1750
- 4 STANDING COMMITTEES
  - ARCHITECTURE
  - STANDARDS
  - SOFTWARE TOOLS
  - VERIFICATION
- MEET 3 TO 4 TIMES PER YEAR
  - HOSTED BY INDUSTRY ORGANIZATIONS
  - 2 DAYS PER MEETING

MIL-STD-1750A HIERARCHY OF DEFINITIONS



MUST BE IMPLEMENTED AS DEFINED (NO SUBSETTING).

IF ENTITY OR FEATURE IS IMPLEMENTED, IT MUST BE AS DEFINED IN THE STANDARD --- PRESERVES SUPPORT SOFTWARE.

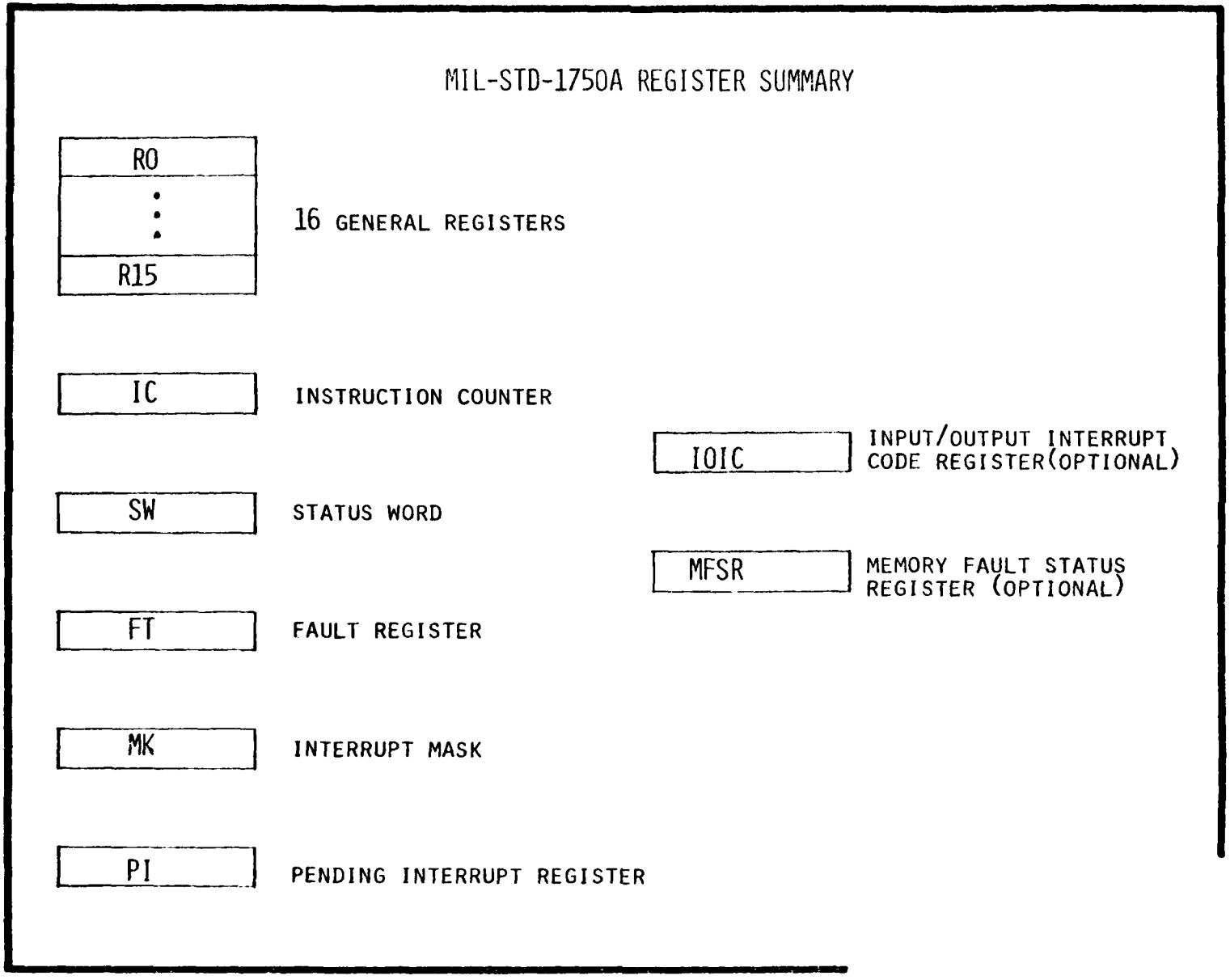
ENTITY DESCRIBED IS SET ASIDE FOR FUTURE DEFINITION--- MUST NOT BE USED (FORBIDDEN) --- RESPONSIBILITY OF MIL-STD- 1750 CONTROL BOARD.

AVAILABLE AS APPROPRIATE FOR IMPLEMENTATION USE.

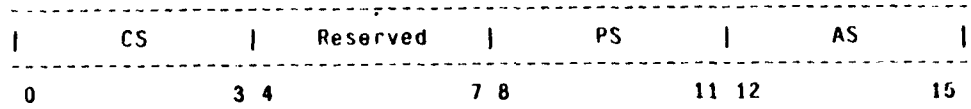
MIL-STD-1750A ISA OVERVIEW

16-BIT GENERAL REGISTER ARCHITECTURE WITH FOLLOWING GENERAL CHARACTERISTICS:

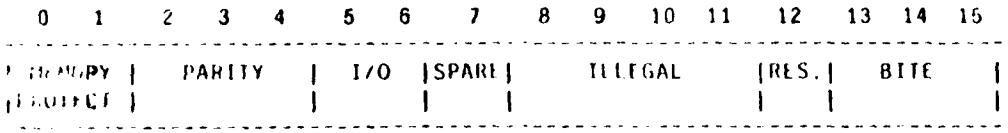
- 16/32-BIT INSTRUCTIONS
- 16/32-BIT FIXED POINT DATA, 32/48-BIT FLOATING POINT DATA
- MULTIPLE ADDRESSING MODES FOR REGISTER, LITERAL, AND MEMORY ACCESS
- 16-BIT ADDRESS RANGE WITH PAGING EXPANSION AND PROTECTION
- BIF INSTRUCTION "EXCAPE/EXPANSION" PROVISION
- FLEXIBLE I/O CONTROL FRAMEWORK
- VECTORED INTERRUPTS AND EXCEPTIONS
- OPTIONAL IMPLEMENTATION PROVISIONS ON SOME FEATURES


MIL-STD-1750A REGISTER SUMMARY
R0
R15
16 GENERAL REGISTERS
IC
INSTRUCTION COUNTER
IOIC
INPUT/OUTPUT INTERRUPT CODE REGISTER(OPTIONAL)
SW
STATUS WORD
MFSR
MEMORY FAULT STATUS REGISTER (OPTIONAL)
FT
FAULT REGISTER
MK
INTERRUPT MASK
PI
PENDING INTERRUPT REGISTER

MIL-STD-1750A STATUS WORD AND FAULT REGISTER FORMATS

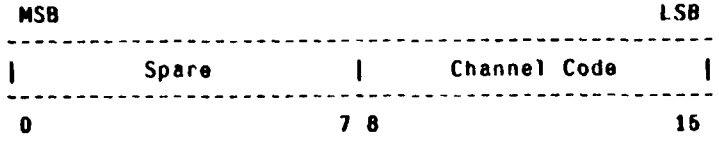


STATUS WORD



FAULT REGISTER

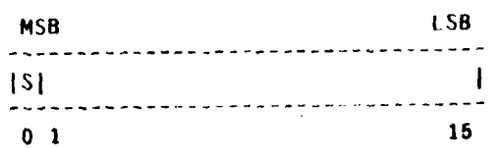
MIL-STD-1750A OPTIONAL REGISTERS



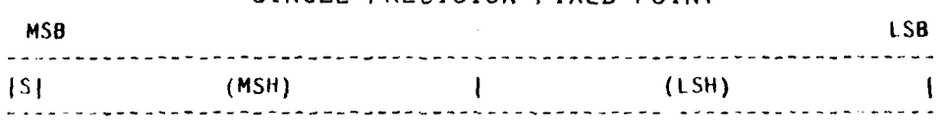
IOIC REG.

MFSR

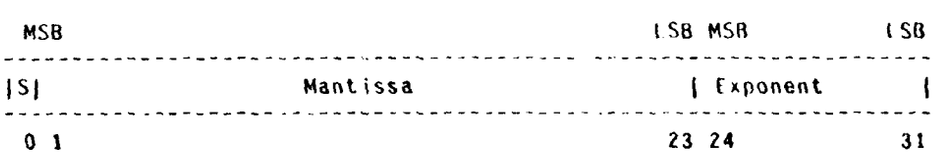
MIL-STD-1750A DATA FORMATS



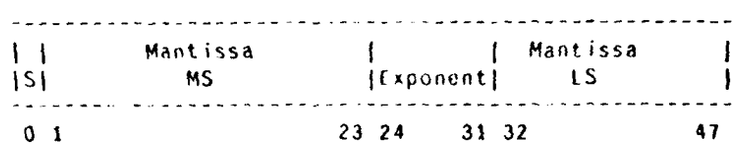
SINGLE PRECISION FIXED POINT



DOUBLE PRECISION FIXED POINT

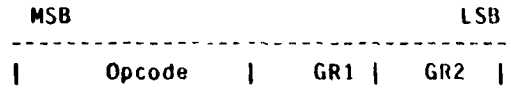


FLOATING POINT

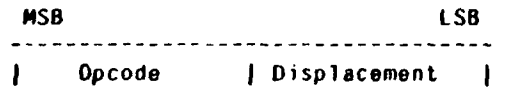


EXTENDED PRECISION FLOATING POINT

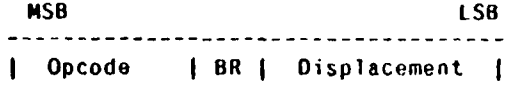
MIL-STD-1750A SHORT INSTRUCTION FORMATS



REGISTER-TO-REGISTER



INSTRUCTION COUNTER RELATIVE



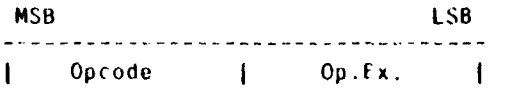
BR = 0 implies general register 12

BR = 1 implies general register 13

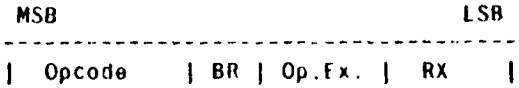
BR = 2 implies general register 14

BR = 3 implies general register 15

BASE RELATIVE



SPECIAL



BR = 0 implies general register 12

BR = 1 implies general register 13

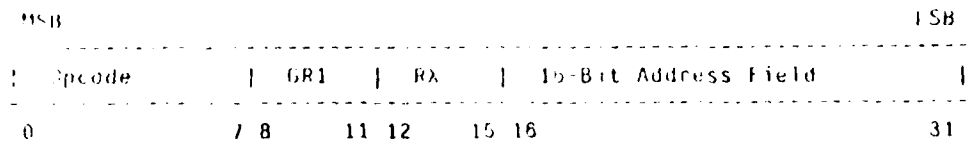
BR = 2 implies general register 14

BR = 3 implies general register 15

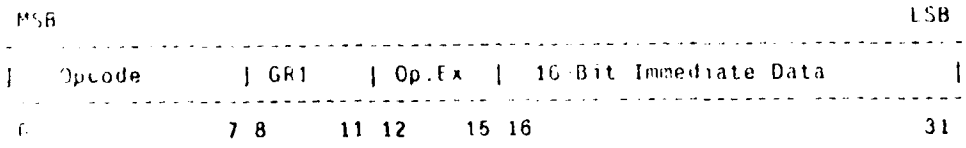
RX = 0 implies no indexing

BAWE RELATIVE INDEXED

MIL-STD-1750A LONG INSTRUCTION FORMATS

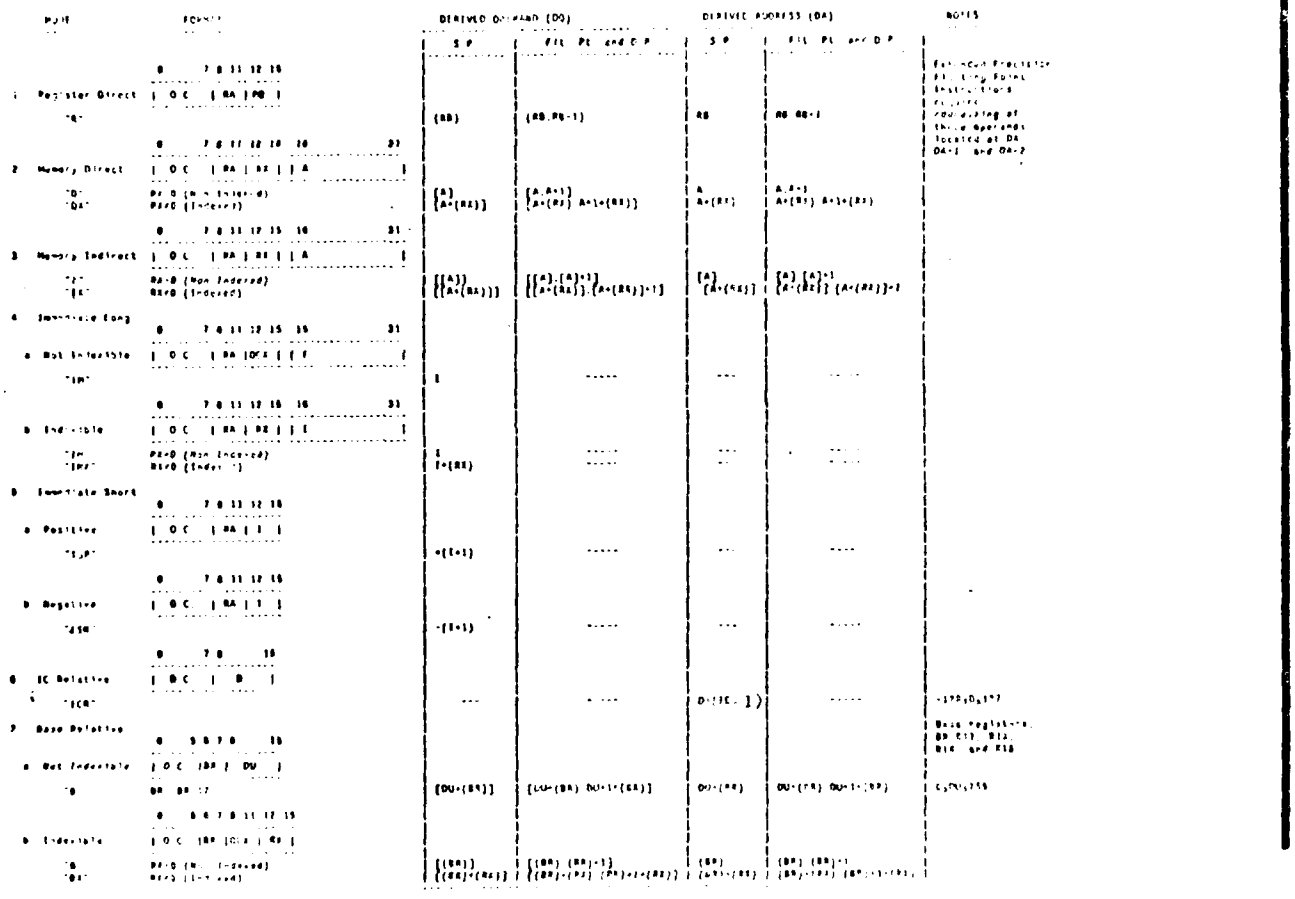


LONG



IMMEDIATE OPCODE EXTENSION

MIL-STD-1750A ADDRESSING MODES



MIL-STD-1750A INTERRUPT DEFINITION TABLE

Interrupt Number	Interrupt Mask Bit Number	Interrupt Linkage Pointer Address (Hex)	Interrupt Service Pointer Address (Hex)	
0	0	20	21	Power Down (cannot be masked or disabled)
1	1	22	23	Machine Error (cannot be disabled)
2	2	24	25	Spare
3	3	26	27	Floating Point Overflow
4	4	28	29	Fixed Point Overflow
5	5	2A	2B	Executive Call (cannot be masked or disabled)
6	6	2C	2D	Floating Point Underflow
7	7	2E	2F	Timer A (if implemented)
8	8	30	31	Spare
9	9	32	33	Timer B (if implemented)
10	10	34	35	Spare
11	11	36	37	Spare
12	12	38	39	Input/Output Level 1 (if implemented)
13	13	3A	3B	Spare
14	14	3C	3D	Input/Output Level 2 (if implemented)
15	15	3E	3F	Spare

Notes: Interrupt number 0 has the highest priority. Priority decreases with increasing interrupt number.

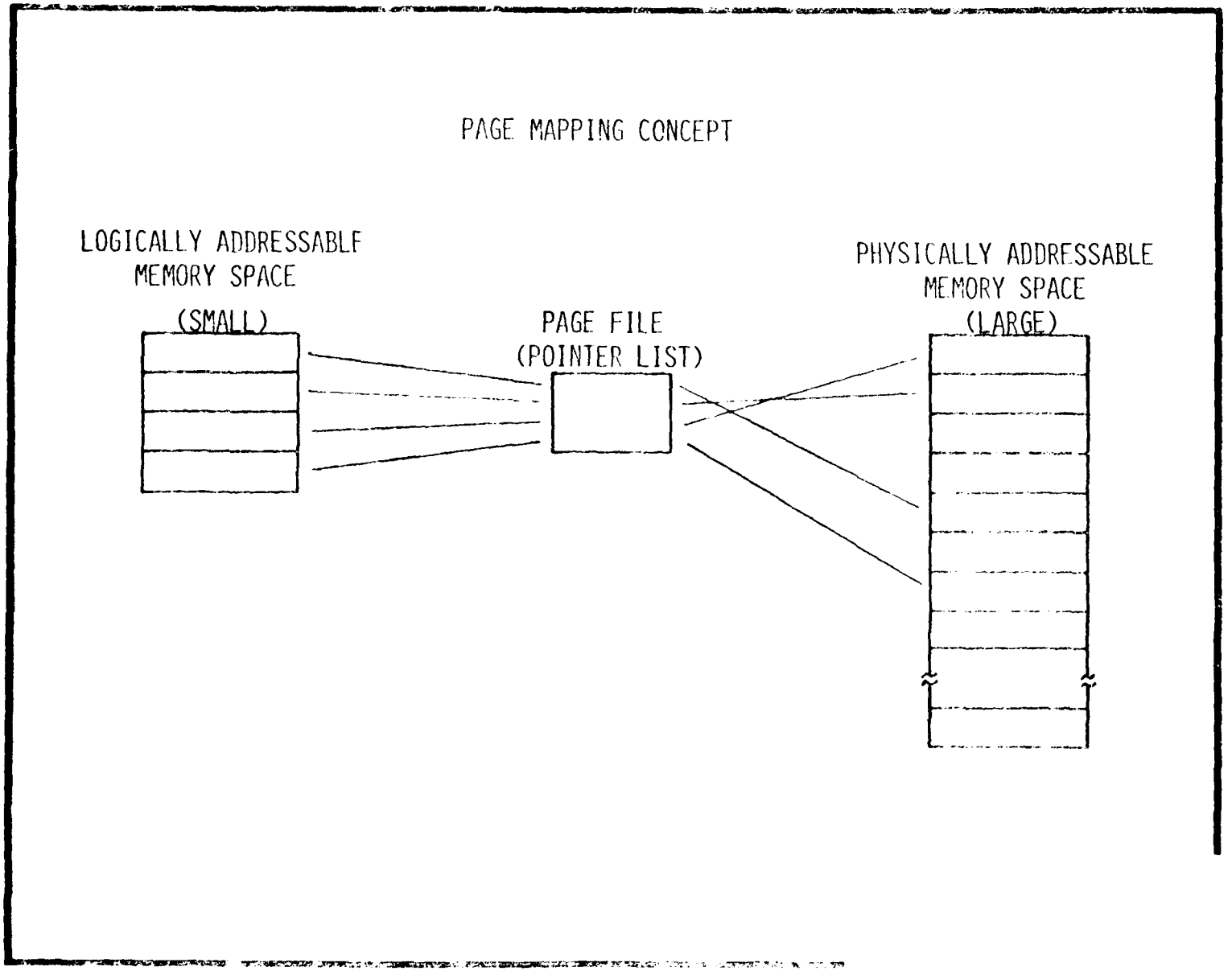
MIL-STD-1750A PROCESSOR RESET STATE DEFINITIONS

Register/Device/Function	Condition After Reset
Instruction Counter	All zeros
Status Word	All zeros
Fault Register	All zeros
Pending Interrupt Register	All zeros
Interrupt Mask Register	All zeros
General Registers	Indeterminate
Interrupts	Disabled
Timers A & B	Started and all zeros [1]
Page Registers	Group 0 enabled [1]
Page Registers AL Field	All zeros [1]
Page Registers W Field	Zero [1]
Page Registers E Field	Zero [1]
Page Registers PPA field	Exact logical to physical [1]
Memory Protect RAM	Disabled and all zeros [1,2]
Start Up ROM	Enabled [1]
DMA Enable	Disabled [1]
Input Discretes	Indeterminate [1]
Trigger Go Indicator	Started [1]
Discrete Outputs	All zeros [1]

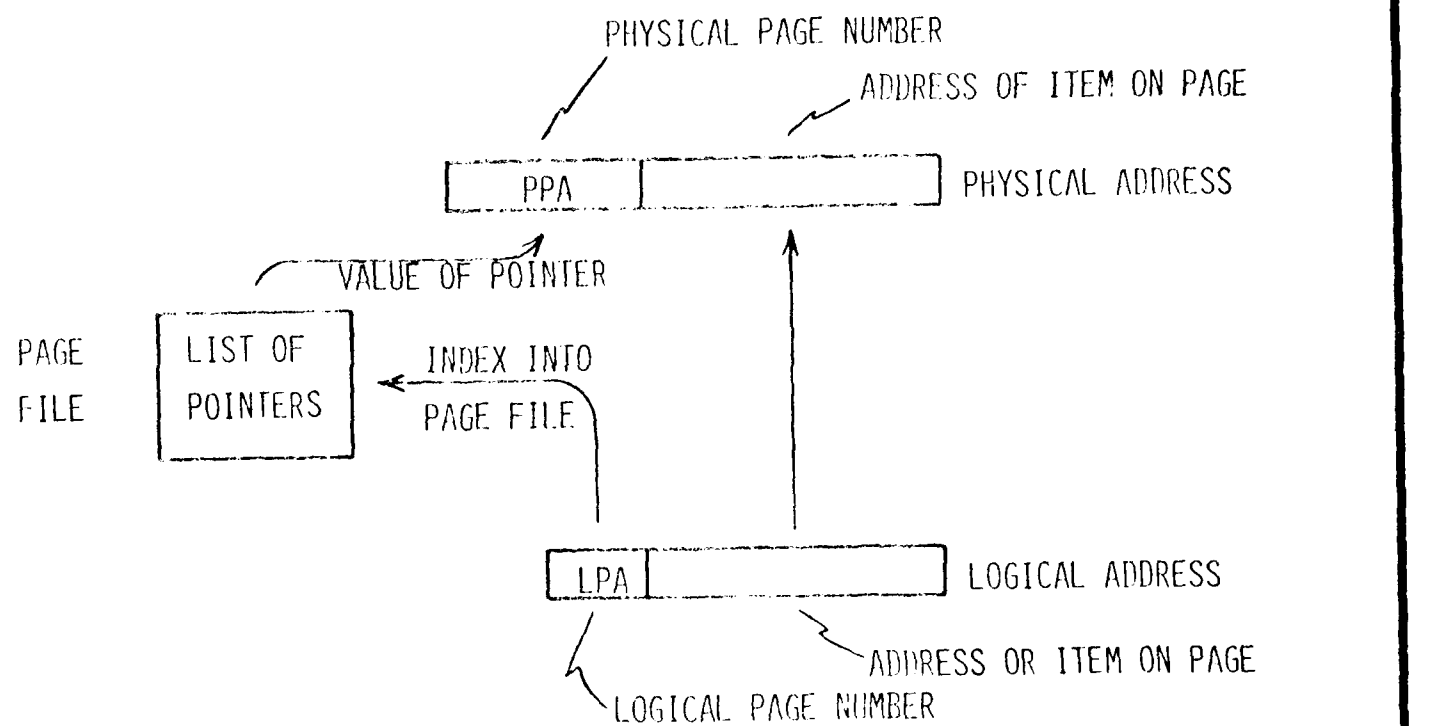
[1] If implemented (optional)
[2] Main Memory Globally Protected

EXPANDED ADDRESSING GENERAL OVERVIEW

- VIRTUAL VS. MAPPED EXPANSION
- PAGING DESIGN TRADE-OFF ISSUES
  - LOGICAL ADDRESS PARTITIONING AND ORGANIZATION
  - INTERRUPT AND SOFTWARE CALL CONTEXT SWITCHING AND INTEGRITY
  - SECURITY AND USAGE PROTECTION
  - PAGE MANAGEMENT SOFTWARE OVERHEAD
  - POWER SEQUENCING AND VOLATILITY ASPECTS AND INTEGRITY
  - SUPPORT SOFTWARE IMPLICATIONS
- PAGE MAPPING MECHANISM


PAGE MAPPING CONCEPT
LOGICALLY ADDRESSABLE
MEMORY SPACE
(SMALL)
PAGE FILE
(POINTER LIST)
PHYSICALLY ADDRESSABLE
MEMORY SPACE
(LARGE)

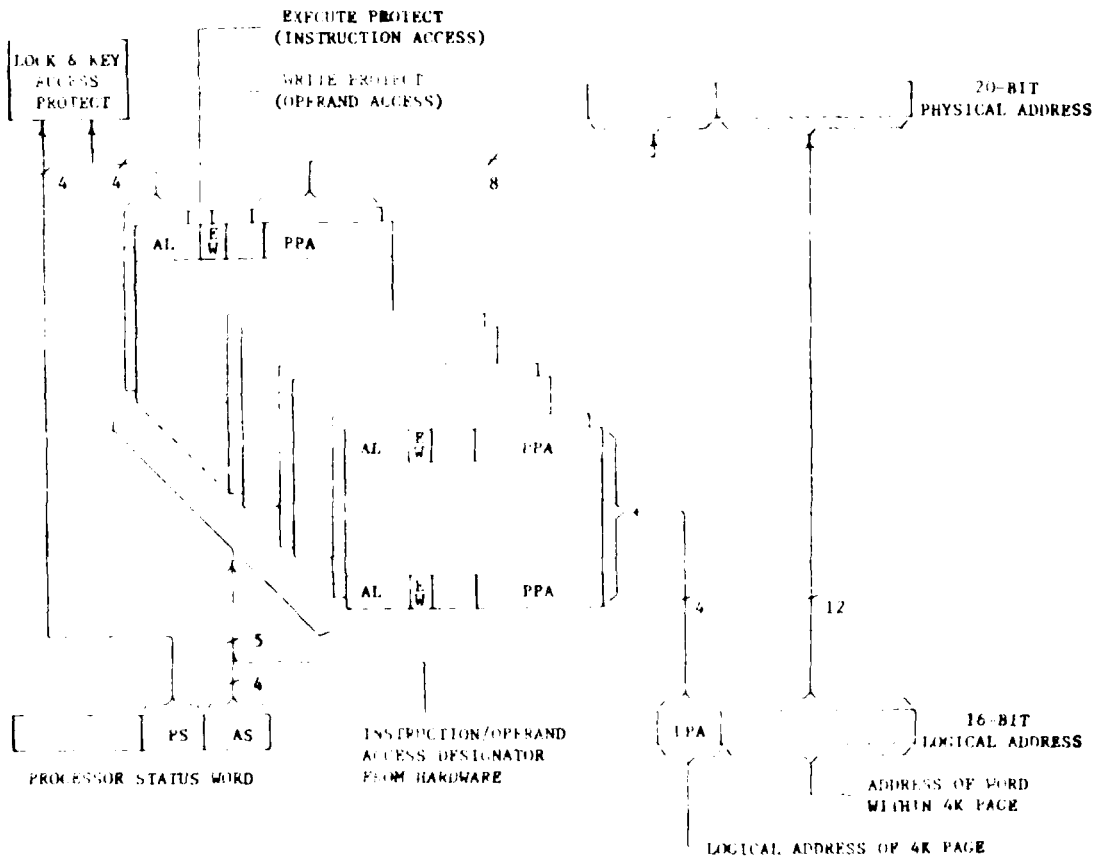
LOGICAL ADDRESS TO PHYSICAL ADDRESS PAGING TRANSLATION PROCESS



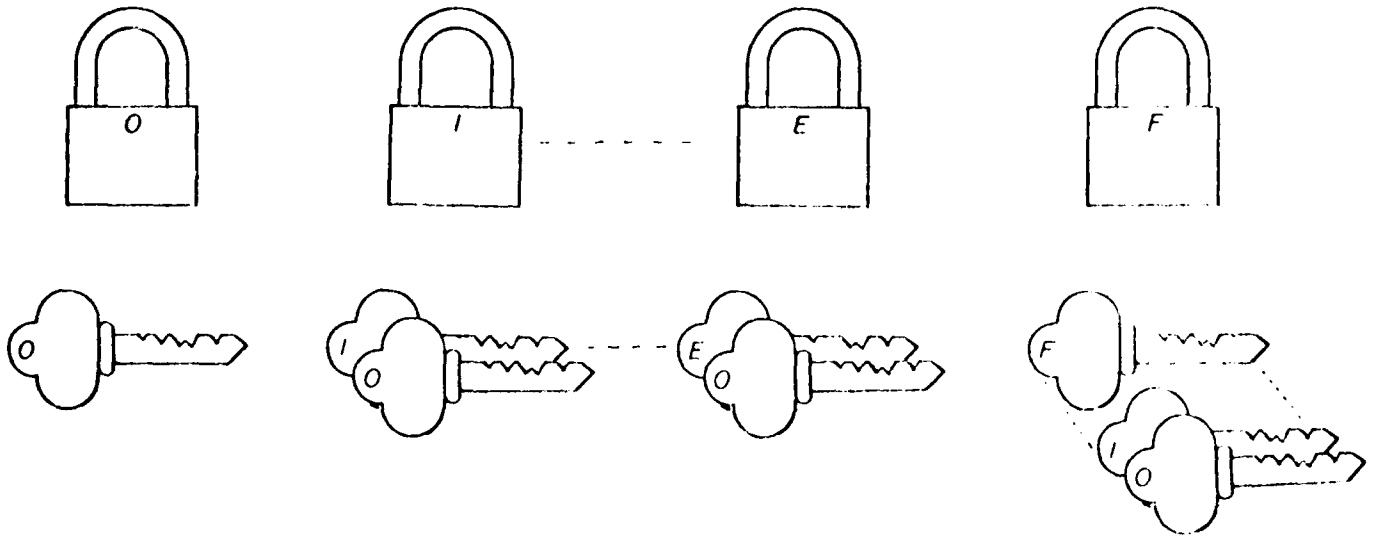
1750A EXPANDED ADDRESSING FEATURES REVIEW

- ORGANIZATION
  - ADDRESS PARTITIONING (4K PAGE SIZE, 20-BIT PHYSICAL ADDRESS)
  - SETS AND GROUPS AND SELECTION
  - FORMATS AND FIELDS
- LOCK AND KEY SCHEME
- INITIALIZATION
- INTERRUPTS AND CONTEXT SWITCHING
- PARTIAL IMPLEMENTATION OPTIONS

1750A ADDRESS PAGING DIAGRAM

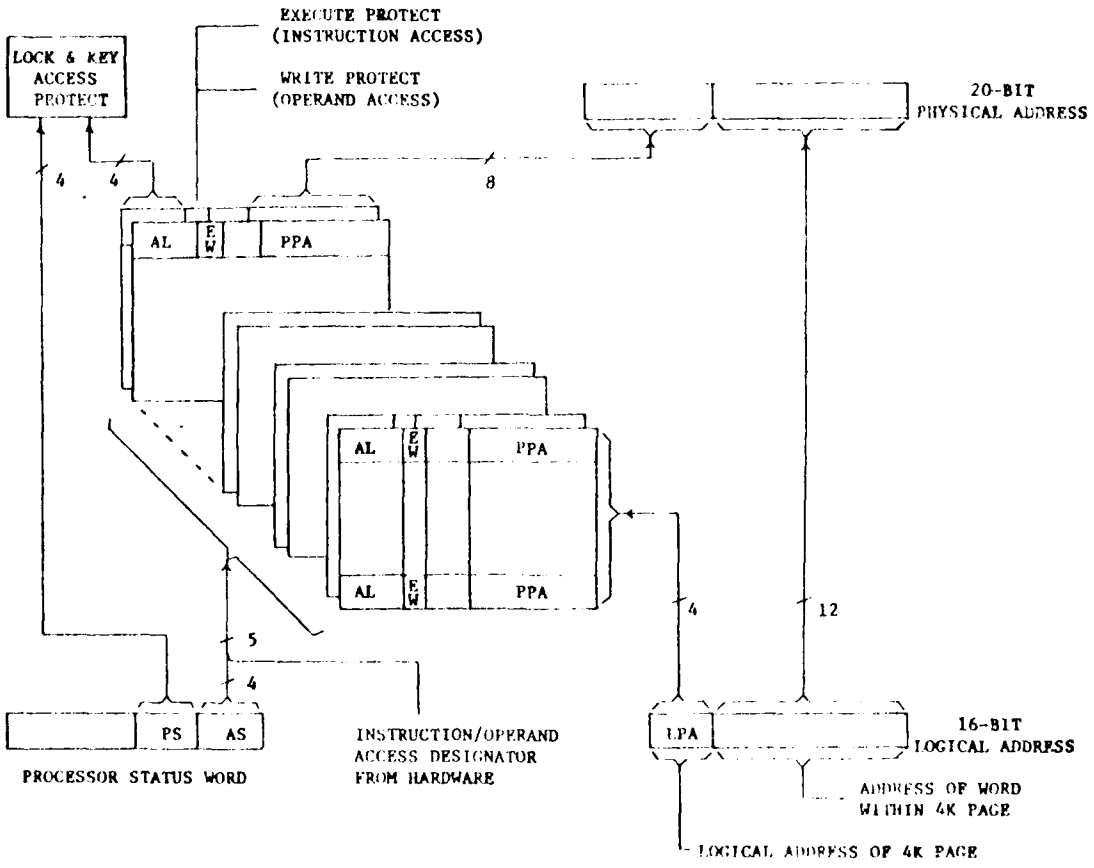


1750A LOCK AND KEY SCHEME

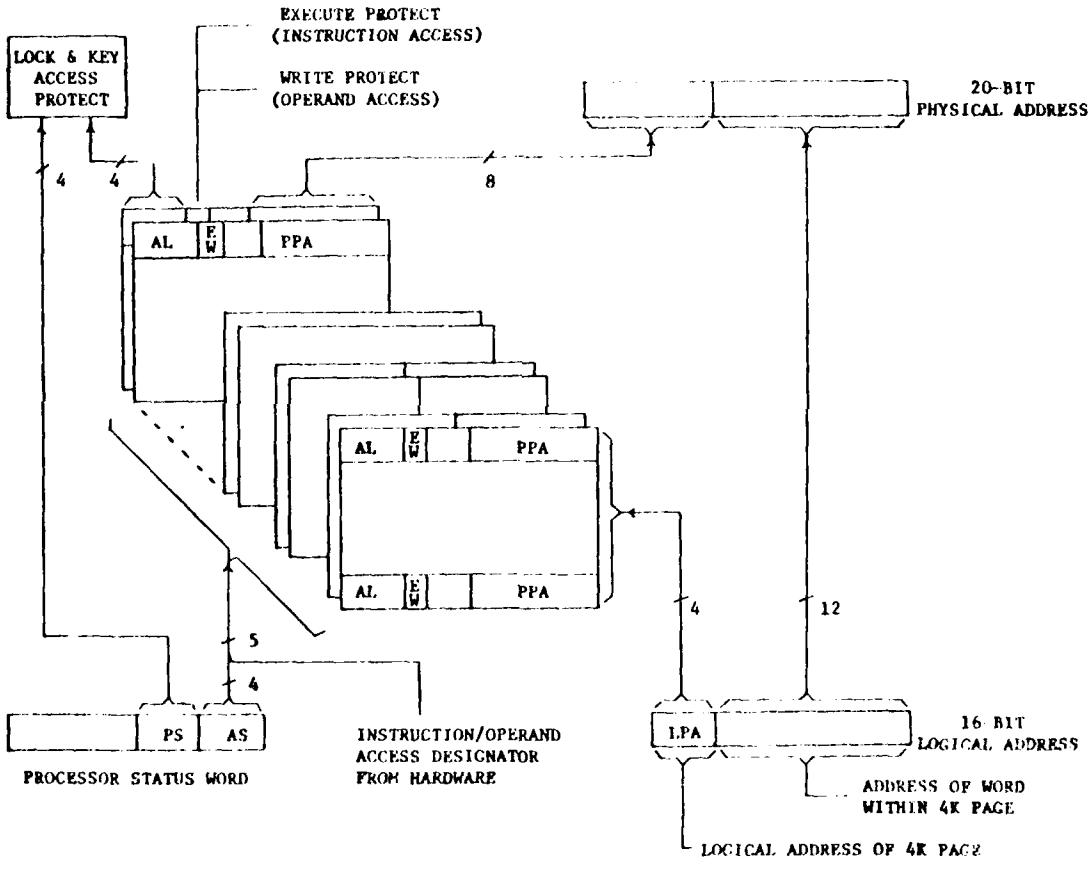


- LOCK 0 AND KEY 0 ARE "MASTER"
- LOCK E IS "COMMON" TO ALL KEYS
- LOCKS 1 THRU E ARE "PRIVATE" TO ASSOCIATED KEY AND KEY 0

1750A PAGING INITIALIZATION

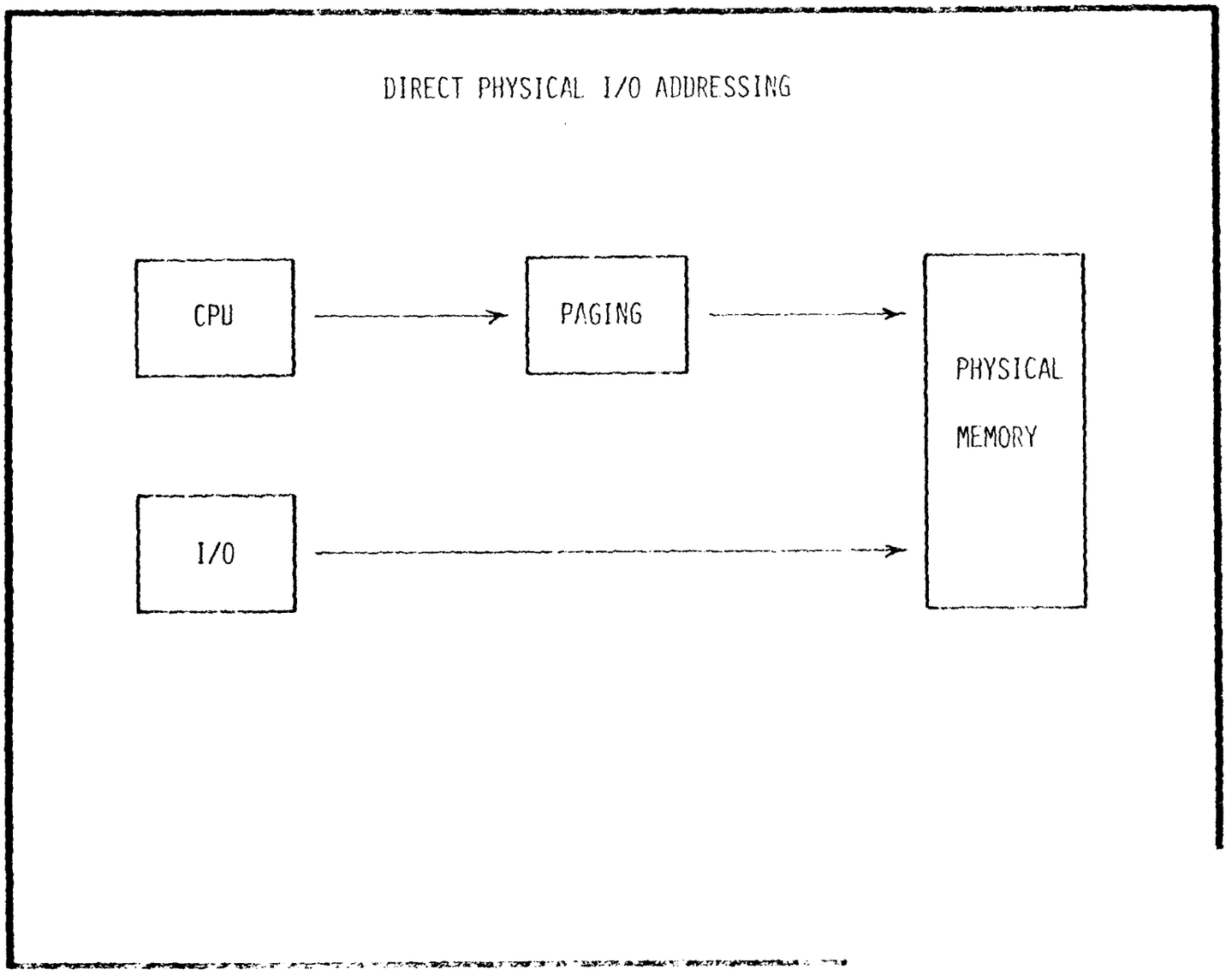


1750A EXPANDED ADDRESSING MINIMUM IMPLEMENTATION

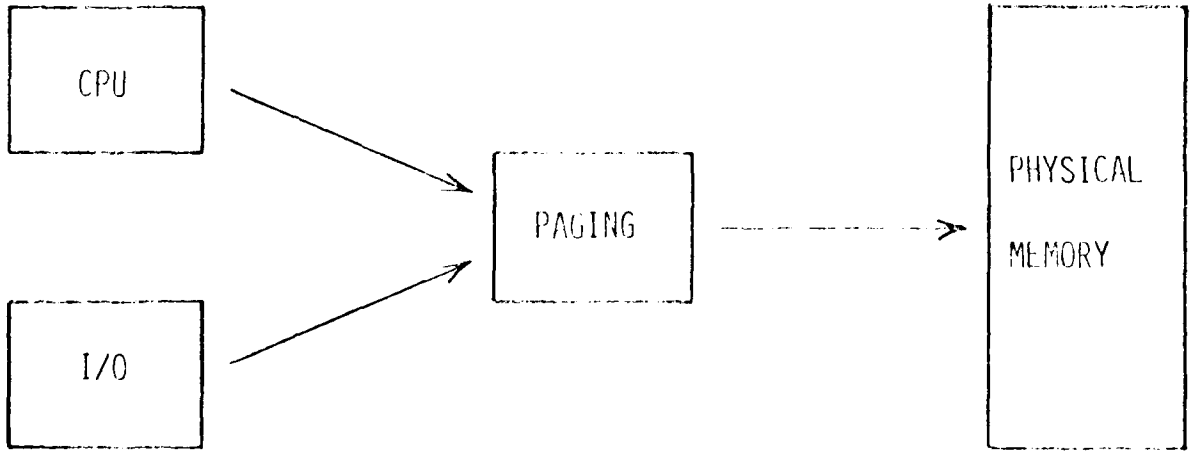


I/O ADDRESSING SCHEMES

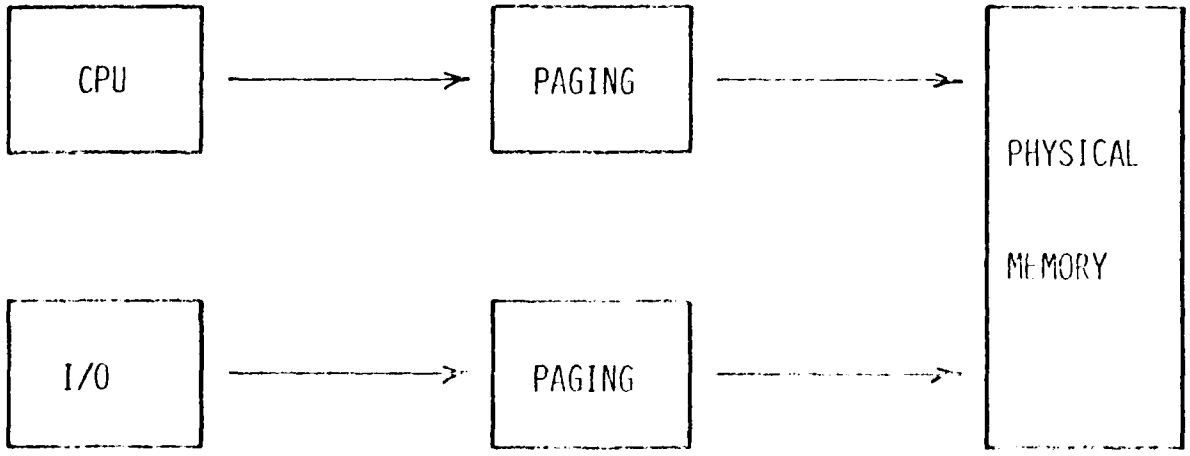
- DIRECT PHYSICAL
- VIA CPU PAGING WITH INDEPENDENT ADDRESS STATE(S) AND KEY(S)
- ADDITIONAL GROUP(S) OF PAGE FILES
- OTHER?


DIRECT PHYSICAL I/O ADDRESSING
CPU
PAGING
PHYSICAL
MEMORY
I/O

COMMON PAGING I/O ADDRESSING



SEPARATE PAGING I/O ADDRESSING



LOCK AND KEY USAGE APPLICABILITY

- NOT "NEED-TO-KNOW" SECURITY
- HARDWARE/SOFTWARE FAULT PROTECTION
- DEBUG/TEST TOOL
- SOFTWARE MAINTENANCE

DEMAND PAGING AND DYNAMIC ALLOCATION

- APPLICABILITY
- "PRECISE INTERRUPT" REQUIREMENTS
- "MODIFIED" OR "WRITE" STATUS BITS

SUPPORT SOFTWARE IMPLICATIONS

- COMPILER
- LOADER/LINKER
- OTHER

MIL-STD-1750A I/O COMMAND SPACE ASSIGNMENTS

Output	Input	Usage
00XX	80XX \	
	>	P10
03XX	83XX /	
04XX	84XX \	
	>	Spare
1FXX	9FXX /	
20XX	A0XX	Processor & Auxiliary Register Control
21XX	A1XX \	
	>	Reserved
2FXX	AFXX /	
30XX	B0XX \	
	>	Spare
3FXX	BFXX /	
40XX	C0XX	Processor & Auxiliary Register Control
41XX	C1XX \	
	>	Reserved
4FXX	CFXX /	
50XX	D0XX	Memory Protect RAM
51XX	D1XX \	
	>	Memory Address Extension
52XX	D2XX /	(page register commands)
53XX	D3XX \	
	>	Spare
7FXX	FFXX /	

MIL-STD-1750A INPUT/OUTPUT INSTRUCTIONS

ADDR MODE	MNEMONIC		FORMAT/OPCODE
IM	XIO	RA,CMD	8 4 4 16
IMX	XIO	RA,CMD,RX	48 RA RX CMD

ADDR MODE	MNEMONIC		FORMAT/OPCODE
D	VIO	RA,ADDR	8 4 4 16
DX	VIO	RA,ADDR,RX	49 RA RX ADDR

DESCRIPTION: The vectored input/output instruction performs the I/O operation as specified by the input/output vector table starting at the derived address, DA, as shown below:

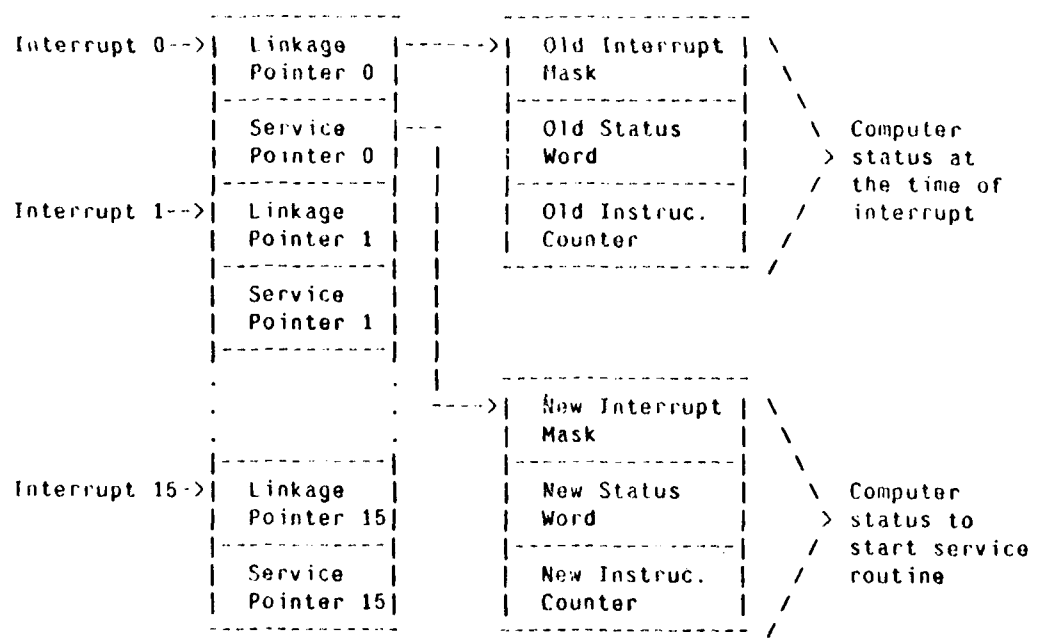
DA	CMD	
DA+1	Vector Select	
DA+2	Data	} one data word for each bit set in the vector select
...	...	

VIO USAGE EXAMPLES

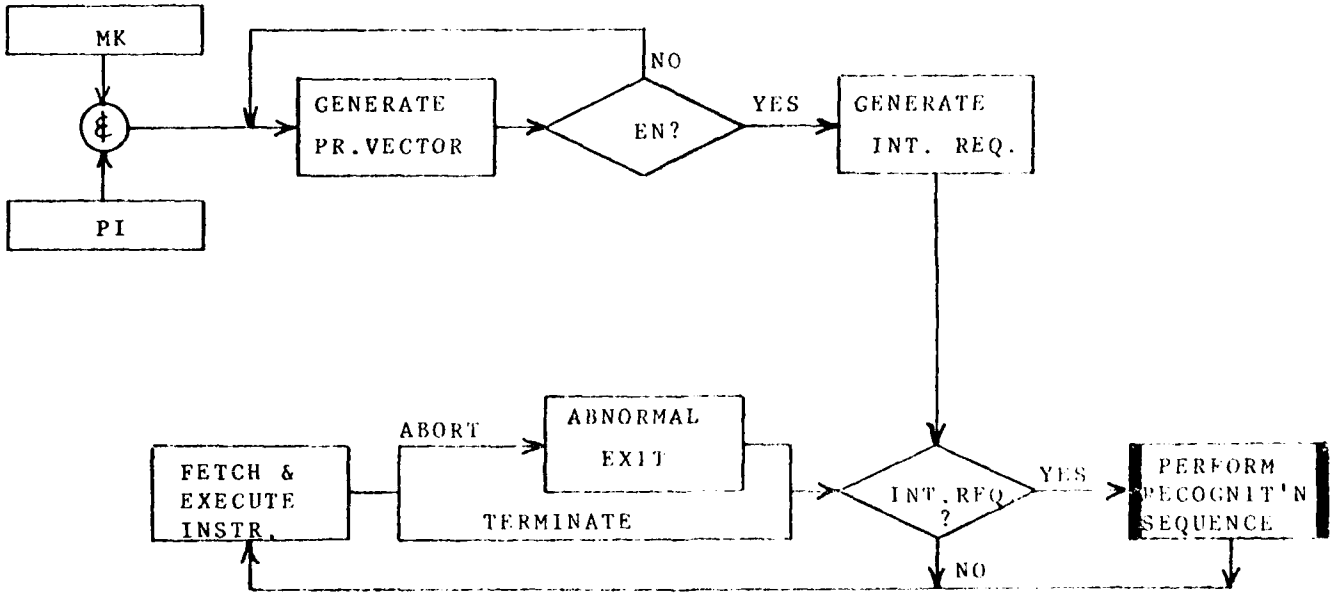
- Block of Commands to Same Device
  - Page Registers
  - Protect RAM
  - I/O Channel Control Registers

- Same Command to Series of Devices
  - Reset Several Devices
  - Initialize Several Devices
  - Enable Interrupts on Several Devices
  - Store Status From Several Devices

MIL-STD-1750A INTERRUPT LINKAGE POINTER AND SERVICE POINTER DEFINITIONS



MIL-STD-1750A INTERRUPT ACTIVITY FLOW DIAGRAM



MIL-STD-1750A INTERRUPT RECOGNITION SEQUENCE

STEP 1. SAVE OLD CONTEXT (MK, SW, AND IC) IN TEMP.

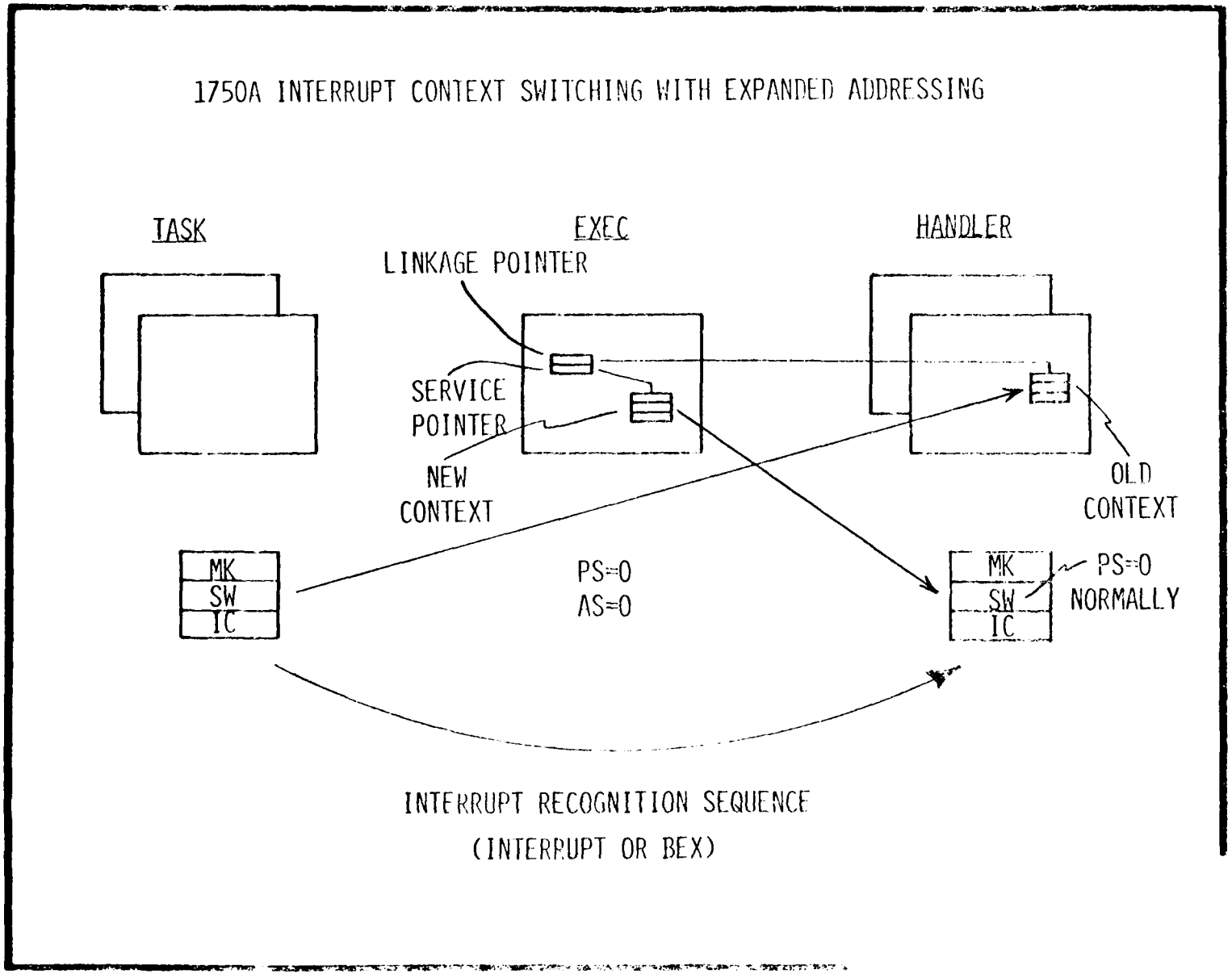
STEP 2. SET PS=0 AND AS=0 IN RESPECTIVE FIELDS OF SW.

STEP 3. FETCH LINKAGE POINTER AND SERVICE POINTER PER PRIORITY INTERRUPT VECTOR.

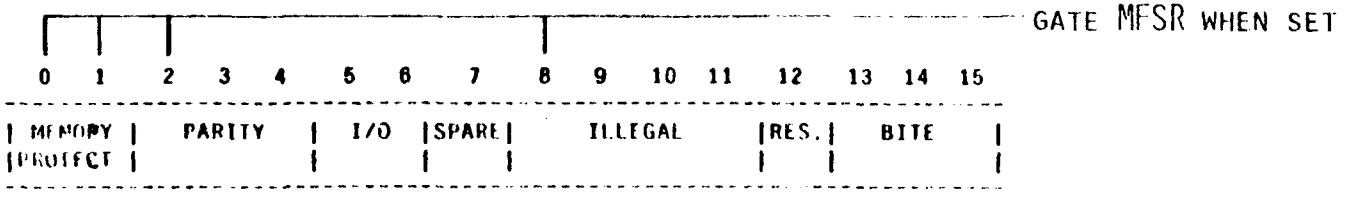
STEP 4. FETCH NEW CONTEXT PER OBTAINED SERVICE POINTER.

STEP 5. ESTABLISH NEW CONTEXT (MK, SW AND IC)

STEP 6. STORE TEMP (OLD CONTEXT) PER OBTAINED LINKAGE POINTER.


1750A INTERRUPT CONTEXT SWITCHING WITH EXPANDED ADDRESSING
TASK
EXEC
HANDLER
LINKAGE POINTER
SERVICE POINTER
NEW CONTEXT
OLD CONTEXT
MK
SW
IC
PS=0
AS=0
MK
SW
IC
PS=0 NORMALLY
INTERRUPT RECOGNITION SEQUENCE
(INTERRUPT OR BEX)

MIL-STD-1750A FAULT REGISTER BIT DEFINITIONS

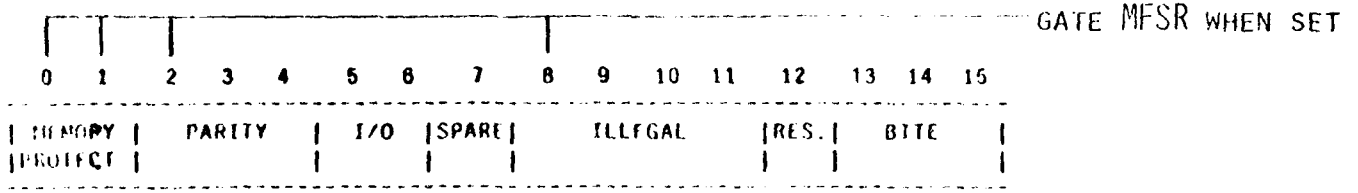


BIT 2: MEMORY PARITY FAULT

BIT 3: PIO CHANNEL PARITY FAULT

BIT 4: DMA CHANNEL PARITY FAULT

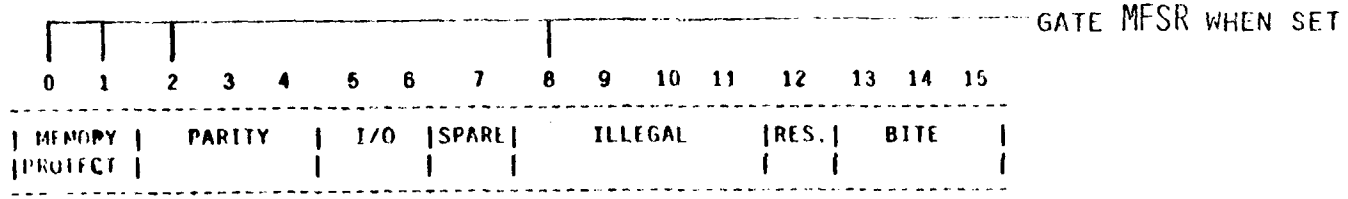
MIL-STD-1750A FAULT REGISTER BIT DEFINITIONS



BIT 5: ILLEGAL I/O COMMAND FAULT. AN ATTEMPT HAS BEEN MADE TO EXECUTE AN UNIMPLEMENTED OR RESERVED I/O COMMAND.

BIT 6: PIQ TRANSMISSION FAULT. OTHER I/O ERROR CHECKING DEVICES, IF USED, MAY BE ORED INTO THIS BIT TO INDICATE AN ERROR.

MIL-STD-1750A FAULT REGISTER BIT DEFINITIONS



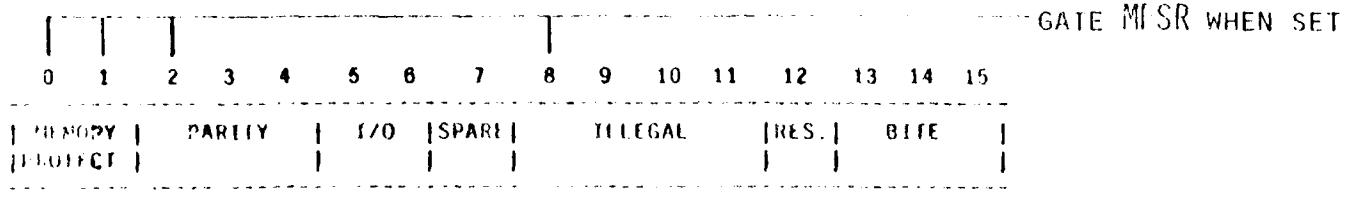
BIT 8: ILLEGAL ADDRESS FAULT. A MEMORY LOCATION HAS BEEN ADDRESSED WHICH IS NOT PHYSICALLY PRESENT.

BIT 9: ILLEGAL INSTRUCTION FAULT. AN ATTEMPT HAS BEEN MADE TO EXECUTE A RESERVED CODE.

BIT 10: PRIVILEGED INSTRUCTION FAULT. AN ATTEMPT HAS BEEN MADE TO EXECUTE A PRIVILEGED INSTRUCTION WITH PS/=0.

BIT 11: ADDRESS STATE FAULT. AN ATTEMPT HAS BEEN MADE TO ESTABLISH AN AS VALUE FOR AN UNIMPLEMENTED PAGE REGISTER SET.

MIL-STD-1750A FAULT REGISTER BIT DEFINITIONS



BIT 13: BUILT-IN TEST FAULT. HARDWARE BUILT-IN TEST EQUIPMENT (BITE) ERROR HAS BEEN DETECTED.

BIT 14-15: SPARE BITE. THESE BITS ARE FOR USE BY THE DESIGNER FOR FUTURE DEFINING (CODING, ETC.) THE BITE ERROR WHICH IS DETECTED. THIS CAN BE USED WITH BIT 13 TO GIVE A MORE COMPLETE ERROR DESCRIPTION.


DATE
ILME